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10/711,181	08/31/2004	Ira Liao	VIAP0128USA	5180

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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,181	LIAO ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-9,11-16,18-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,11-16,18-20 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on December 13, 2006 was filed after the mailing date of the application on August 31, 2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. Applicant's arguments with respect to claims 1-5, 7-9, 11-16, 18-20, and 22 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, see page 7, filed November 20, 2006, with respect to the rejection(s) of claim(s) 1-5, 7-9, 11-16, 18-20, and 22 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sato (US006469748B1).

4. Applicant argues that MacInnis teaches that video data will be downscaled before capturing video frame to memory. In contrast, the claims invention teaches that the digital video signal is directly transmitted from the video capture engine to the memory without downscaling (page 7).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Sato.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1) in view of Jackson (US005544202A), further in view of Sato (US006469748B1).

8. With regard to Claim 1, MacInnis describes a graphics card (10, Figure 1; *graphics display system contained in an integrated circuit 10*, Col. 5, lines 8-10) for smoothing the

playing of video (*clock switching may be done without causing glitches on the display side*, Col. 29, lines 64-66). The graphics card includes inputs (12, Figure 1) for receiving video signals (14; Col. 5, lines 10-11), as shown in Figure 1, and also shown in Figure 2 as digital video in which is input to the mux (Col. 5, lines 54-56), and therefore the graphics card must inherently have a video capture engine for receiving the digital video signal. A video scaler (52) is connected to the video capture engine, as shown in Figure 2, and a memory (28, Figure 1) is connected to the video scaler for storing the digital signal captured by the video capture engine (*video scaler downscales before capturing video frames to memory*, Col. 6, lines 16-17). Figure 5 shows a video DMA 144 that transfers the captured video frames to a video FIFO 148 from the external SDRAM to the video scaler 52 (Col. 12, lines 8-15). The video scaler processes the digital video signal (Col. 12, lines 11-15) and stores the video data in the memory (Col. 6, lines 15-17), and the video display engine (58) receives the video data from memory that was stored as digital video data (Col. 10, lines 51-59). Therefore, the video scaler is a video process engine that is connected to the memory for processing the digital video signal of the memory into digital video data and then storing the digital video data in the memory. A video display engine (58, Figure 2) is connected to the memory for receiving the digital signal or the digital video data stored in the memory (*display engine 58 takes graphics information from memory and processes it for display*, Col. 7, lines 3-4); and a first clock generator connected to the video capture engine and the video display engine for providing the same clock to the video capture engine and the video display engine so as to synchronize the signal receiving rates of the video capture engine and the video display engine (*video input which runs nominally at 13.5 MHZ is synchronized with the display clock which runs nominally at 13.5 MHZ at the output*, Col. 11, lines 59-67).

However, MacInnis does not teach providing the same clock having the same frequency and the same phase to the video capture engine and the video display engine. However, Jackson describes providing the same clock having the same frequency and the same phase to the video capture engine and the video display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of MacInnis to include providing the same clock having the same frequency and the same phase to the video capture engine and the video display engine as suggested by Jackson because Jackson suggests that this is needed in order to synchronize the display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3).

However, MacInnis and Jackson do not teach that the memory stores the digital video signal without downscaling the digital video signal. However, Sato discloses a video signal capturing apparatus (9, Figure 2) for receiving a video signal and converting it to a digital video signal; a memory connected to the video signal capturing apparatus for storing the digital signal captured by the video capture engine without downscaling the digital video signal; and an external processing apparatus connected to the memory for receiving the digital signal or the digital video data stored in the memory (Col. 2, lines 30-37). According to the disclosure of this application, this invention teaches transforming a received analog video signal into a digital video signal, and the video capture engine receives the digital video signal and stores the digital video signal in memory [Para 13]. Therefore, the video signal capturing apparatus of Sato is similar to the video capture engine of this invention.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of MacInnis and Jackson so that the memory stores the digital

video signal without downscaling the digital video signal as suggested by Sato because Sato suggests the advantage of directly capturing the signal into the memory (Col. 4, lines 61-64), and then performing operations on the signal that is stored in the memory so that different operations can be performed on the signal depending on where the signal will be sent to (the CPU 1 or the printer mechanism 17) (Col. 5, lines 14-26).

9. With regard to Claim 2, MacInnis describes a decoder (50, Figure 2) connected to the mux which receives digital video in inherently from the video capture engine (Col. 5, lines 46-56), as shown in Figure 2. The decoder is for transforming a received analog video signal into the digital video signal (*video decoder digitizes and processes analog input video*, Col. 5, lines 64-67) and outputting the digital video signal to the mux, as shown in Figure 2, which is inherently connected to the video capture engine.

10. With regard to Claim 3, MacInnis describes that the first clock generator is located in the decoder (50; Col. 11, lines 59-64; Col. 37, lines 8-17).

11. With regard to Claim 4, MacInnis describes an encoder (62, Figure 2) connected to the video compositior (60; *video encoder 62 encodes the blended video output from the video compositor*, Col. 7, lines 20-25), which is connected to the video display engine (58; Col. 7, lines 3-20).

12. With regard to Claim 5, MacInnis describes that the first clock generator is further connected to the encoder (62, Figure 2) for providing the same clock to the video capture engine, the video display engine (58) (Col. 11, lines 59-64), and the encoder (*samples taken for YUV are synchronized to a display clock for compositing with graphics data at the video compositor*, Col. 34, lines 36-38; *video encoder 62 encodes the blended video output from the video compositor*, Col. 7, lines 20-25).

However, MacInnis does not teach providing the same clock having the same frequency and the same phase. However, Jackson describes providing the same clock having the same frequency and the same phase to the video capture engine and the video display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3). This would be obvious for the same reasons given in the rejection for Claim 1.

13. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1), Jackson (US005544202A), and Sato in view of Chih (US006535217B1).

14. With regard to Claim 7, MacInnis, Jackson, and Sato are relied upon for the teachings as discussed above relative to Claim 1.

However, MacInnis, Jackson, and Sato do not specifically teach an output interface connected to the video display engine for outputting the digital video from the video display engine. However, Chih describes an output interface (24, Figure 1) connected to the video display engine (22) for outputting the digital video from the video display engine (*LCD display interface 24 that receives the digital video data from the display engine 22*, Col. 4, lines 19-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of MacInnis, Jackson, and Sato to include an output interface connected to the video display engine for outputting the digital video from the video display engine as suggested by Chih because Chih suggests that an interface is needed to provide a high rate of data transmission and provide transmission capabilities that are reliable and also do not interfere with other elements internal to and external to the computing system (Col. 1, lines 21-27).

15. With regard to Claim 9, MacInnis does not teach that the output interface is a liquid crystal display output (LCD) interface. However, Chih describes that the output interface (24, Figure 1) is a LCD output interface (Col. 4, lines 19-24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of as MacInnis so that the output interface is a liquid crystal display output (LCD) interface as suggested by Chih because Chih suggests that interfaces are especially needed for LCD's because the data rates required to adequately drive an LCD display are very high. When this data is transmitted in a digital fashion, the high-speed switching of the signal lines can result in electromagnetic interference that can have detrimental effects on other portions of the system, and therefore an interface is needed to meet these transmission needs (Col. 1, lines 21-34).

16. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1), Jackson (US005544202A), and Sato (US006469748B1) in view of Van Hook (US006867781B1).

17. With regard to Claim 7, MacInnis, Jackson, and Sato are relied upon for the teachings as discussed above relative to Claim 1.

However, MacInnis, Jackson, and Sato do not specifically teach an output interface connected to the video display engine for outputting the digital video from the video display engine. However, Van Hook describes an output interface (164, Figure 4) connected to the video display engine (180, 114) for outputting the digital video from the video display engine (*output of graphics pipeline 180 is read each frame by display/video interface unit 164, display controller/video interface 164 provides digital RGB pixel values for display*, Col. 7, lines 58-62). This would be obvious for the same reasons given in Chih, as discussed above.

18. With regard to Claim 8, MacInnis describes that the first clock generator provides the same clock to the video capture engine and the video display engine (58; Col. 11, lines 59-64).

However, MacInnis does not teach that the first clock generator is further connected to the output interface for also providing the same clock to the output interface. However, Van Hook describes providing a mechanism to synchronize the video display engine (114, Figure 4) and the output interface (164) (Col. 7, line 63-Col. 8, line 5), and therefore Van Hook inherently discloses a first clock generator that is connected to the output interface for providing the same clock to the video display engine and the output interface.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of MacInnis so that the first clock generator is further connected to the output interface for also providing the same clock to the output interface as suggested by Van Hook because Van Hook suggests that it is often desirable to synchronize these different stages of the rendering system to establish time-coherence between various operations. For example, it would be very useful for the graphics command producer to known under certain circumstances when the graphics processor has finished processing a given graphics command (Col. 1, lines 47-63). Synchronizing these components allows for various programming model with different levels of complexity (Col. 7, line 63-Col. 8, line 5).

However, MacInnis and Van Hook do not teach providing the same clock having the same frequency and the same phase. However, Jackson describes providing the same clock having the same frequency and the same phase to the video capture engine and the video display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3). This would be obvious for the same reasons given in the rejection for Claim 1.

19. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1), Jackson (US005544202A), and Sato (US006469748B1) in view of Christopher (US006900845B1).

MacInnis, Jackson, and Sato are relied upon for the teachings as discussed above relative to Claim 1.

However, MacInnis, Jackson, and Sato do not teach a video process clock generator connected to the video process engine for providing a clock to the video process engine.

However, Christopher describes a video process clock generator connected to the video process engine (28, 30, 16, Figure 2A) for providing a clock to the video process engine (Col. 6, lines 40-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of MacInnis, Jackson, and Sato to include a video process clock generator connected to the video process engine for providing a clock to the video process engine as suggested by Christopher because Christopher suggests that the video process engine must synchronize with the memory to achieve the desired bandwidth (Col. 6, lines 40-45).

20. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1) in view of Kim (US006738417B1), further in view of Jackson (US005544202A), further in view of Sato (US006469748B1).

21. With regard to Claim 12, MacInnis describes a graphics card (10, Figure 1; *graphics display system contained in an integrated circuit 10*, Col. 5, lines 8-10) for smoothing the playing of video (*clock switching may be done without causing glitches on the display side*, Col. 29, lines 64-66). The graphics card includes inputs (12, Figure 1) for receiving video signals (14; Col. 5, lines 10-11), as shown in Figure 1, and also shown in Figure 2 as digital video in which is input to the mux (Col. 5, lines 54-56), and therefore the graphics card must inherently have a video capture engine for receiving the digital video signal. A video scaler (52) is connected to the video capture engine, as shown in Figure 2, and a memory (28, Figure 1) is connected to the video scaler for storing the digital signal captured by the video capture engine

(*video scaler downscales before capturing video frames to memory*, Col. 6, lines 16-17). Even though MacInnis teaches that video data is downscaled before capturing video frames to memory, downscaling is not necessarily considered to be "special processing," and therefore the video signal is captured in the memory without special processing. Figure 5 shows a video DMA 144 that transfers the captured video frames to a video FIFO 148 from the external SDRAM to the video scaler 52 (Col. 12, lines 8-15). The video scaler processes the digital video signal (Col. 12, lines 11-15) and stores the video data in the memory (Col. 6, lines 15-17), and the video display engine (58) receives the video data from memory that was stored as digital video data (Col. 10, lines 51-59). Therefore, the video scaler is a video process engine that is connected to the memory for processing the digital video signal of the memory into digital video data and then storing the digital video data in the memory. A video display engine (58, Figure 2) connected to the memory for receiving the digital signal of the digital video data stored in the memory (*display engine 58 takes graphics information from memory and processes it for display*, Col. 7, lines 3-4); a first clock generator connected to the video capture engine for providing a first clock to the video capture engine; and a second clock generator connected to the first clock generator to generate a second clock, the second clock having substantially the same frequency as the first clock and being offset from the first clock by a predetermined phase difference (Col. 11, line 59-Col. 12, line 4).

However, MacInnis does not teach a multiplexer having an output connected to the video display engine; and that the first clock generator is connected to a first input of the multiplexer for providing a first clock to the first input of the multiplexer; and that the second clock generator is connected to a second input of the multiplexer. However, Kim describes a

multiplexer (33, Figure 7) having an output connected to the video display engine (graphics controller); and that the first clock generator (external oscillator clock) is connected to a first input of the multiplexer for providing a first clock to the first input of the multiplexer; and that the second clock generator (pixel clock) is connected to a second input of the multiplexer (Col. 4, lines 44-53), the second clock having substantially the same frequency as the first clock and being offset from the first clock by a predetermined phase difference (Col. 4, lines 61-64).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of MacInnis to include a multiplexer having an output connected to the video display engine; and that the first clock generator is connected to a first input of the multiplexer for providing a first clock to the first input of the multiplexer; and that the second clock generator is connected to a second input of the multiplexer as suggested by Kim because Kim suggests that a multiplexer is needed to switch the clocks used in order to absorb the jitter (Col. 4, lines 61-64).

However, MacInnis and Kim do not teach that the first clock is provided to the video capture engine having the same frequency and the same phase as the first clock provided to the first input of the multiplexer. However, Jackson describes providing the same clock having the same frequency and the same phase to the video capture engine and the video display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3). Since Kim teaches that the multiplexer has an output connected to the video display engine, it would be obvious to modify the device of Kim with the teachings of Jackson so that the first clock is provided to the video capture engine having the same frequency and the same phase as the first clock provided to the first input of the multiplexer. This would be obvious for the same reasons given in the rejection for Claim 1.

However, MacInnis, Jackson, and Kim do not teach that the memory stores the digital video signal without downscaling the digital video signal. However, Sato discloses a video signal capturing apparatus (9, Figure 2) for receiving a video signal and converting it to a digital video signal; a memory connected to the video signal capturing apparatus for storing the digital signal captured by the video capture engine without downscaling the digital video signal; and an external processing apparatus connected to the memory for receiving the digital signal or the digital video data stored in the memory (Col. 2, lines 30-37). According to the disclosure of this application, this invention teaches transforming a received analog video signal into a digital video signal, and the video capture engine receives the digital video signal and stores the digital video signal in memory [Para 13]. Therefore, the video signal capturing apparatus of Sato is similar to the video capture engine of this invention. This would be obvious for the same reasons given in the rejection for Claim 1.

22. With regard to Claims 13-15, these claims are similar in scope to Claims 2-4 respectively, and therefore are rejected under the same rationale.

23. With regard to Claim 16, MacInnis describes providing the same clock to the video display engine (58, Figure 2) and the encoder (62) (Col. 11, lines 59-64; Col. 34, lines 36-38; Col. 7, lines 20-25).

However, MacInnis does not teach that a multiplexer is used. However, Kim describes that a multiplexer (33, Figure 7) is used to provide clock signals (Col. 4, lines 44-53), as discussed in the rejection for Claim 12.

However, MacInnis and Kim do not teach providing the same clock having the same frequency and the same phase. However, Jackson describes providing the same clock having the same frequency and the same phase to the video capture engine and the video display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3). This would be obvious for the same reasons given in the rejection for Claim 1.

24. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1), Kim (US006738417B1), Jackson (US005544202A), and Sato (US006469748B1) in view of Van Hook (US006867781B1).

25. With regard to Claim 18, Claim 18 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

26. With regard to Claim 19, MacInnis does not teach providing the same clock to the video display engine and the output interface. However, Van Hook describes providing a mechanism to synchronize the video display engine (114, Figure 4) and the output interface (164) (Col. 7, line 63-Col. 8, line 5), and therefore Van Hook inherently provides the same clock to the video display engine and the output interface, as discussed in the rejection for Claim 8.

However, MacInnis and Van Hook do not teach that a multiplexer is used. However, Kim describes that a multiplexer (33, Figure 7) is used to provide clock signals (Col. 4, lines 44-53), as discussed in the rejection for Claim 12.

However, MacInnis, Van Hook, and Kim do not teach providing the same clock having the same frequency and the same phase. However, Jackson describes providing the same clock having the same frequency and the same phase to the video capture engine and the video display (Col. 1, lines 9-19; Col. 1, line 61-Col. 2, line 3). This would be obvious for the same reasons given in the rejection for Claim 1.

27. Claims 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1), Kim (US006738417B1), Jackson (US005544202A), and Sato (US006469748B1) in view of Chih (US006535217B1).

28. With regard to Claims 18 and 20, these claims are similar in scope to Claims 7 and 9 respectively, and therefore are rejected under the same rationale.

29. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006573905B1), Kim (US006738417B1), Jackson (US005544202A), and Sato (US006469748B1) in view of Christopher (US006900845B1).

With regard to Claim 22, Claim 22 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER